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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,831	12/30/2003	Kevin M. Conley	SNDK.247US0	9380

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,831	CONLEY ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *5-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/6/05,5/14/04*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-4, drawn to a method of writing data into a non-volatile memory by responding to host commands in order write units of data into one of two blocks based on the sequence of logical addresses of the units, classified in class 711, subclass 103.

   II. Claims 5-7, drawn to a method to write data of pages into one of two blocks based on a number sequential logical addresses relative to a predetermined number, classified in class 711, subclass 218.

   III. Claims 8-19, drawn to a method to write data of pages into one of two blocks based on satisfying a predefined condition of data update, classified in class 711, subclass 103.

   IV. Claims 20-25, drawn to a memory and memory system that designates data into one of two blocks based on the address offset of physical locations, classified in class 711 subclasses 103, 218.

2. Inventions I, II, III and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, invention I has separate utility from inventions II, III and IV such as a system that is capable of writing data to two district regions of memory depending if the data is to be stored either randomly or

sequentially. Invention II has separate utility from inventions I, III and IV such as within a system for paging data sequentially based on addresses relative to a predetermined number. Invention III has separate utility from inventions I, II and IV such as within a system that is capable tracking when to store pages of data by determining if the data to be paged has been updated or not. Invention IV has separate utility from inventions II, III and IV such as in a system that can store data based on address offset of physical data locations. See MPEP § 806.05(d).

3. Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

4. A telephonic interview was held with Mr. Gerald Parsons on 15 March 2006 to address the restriction requirement described under paragraphs 1-3 of this correspondence. During the interview, Mr. Parson elected Group I for examination with traverse. The remaining claims derived from Groups II-IV (i.e. claims 5-25) have been withdrawn from further consideration.

Information Disclosure Statement

5. The two information disclosure statements (IDS) submitted on 6 June 2005 and 14 May 2004 were fully considered by the examiner.

Drawings

6. The drawings received on 12 May 2004 are objected to because of the following reason:

Figures 3-7 (including both 7A and 7B) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The abstract of the disclosure is objected to because of the following reasons:

The abstract exceeds the maximum of 150 words.

All extraneous markings (i.e. "Attorney Docket ... SNDK.247US0") should be removed from the abstract.

Correction is required. See MPEP § 608.01(b).

8. The disclosure is objected to because of the following informalities:

There is no reference to Figs. 15A and 15B in the brief description of the drawings (see paragraph 0032 of the original specification).

Appropriate correction is required.

9. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

10. Claims 2-4 are objected to because of the following informalities:

As for claim 2, the phrase "writing the data" as recited in line 5 of this claim should be changed to "writing data".

Claims 3-4 are further objected to for depending on claim 2

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US PG Publication 2002/0099904 A1).

As for claim 1, Conley teaches a method of programming data into a reprogrammable non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data (paragraph 0062, all lines), comprising:

responding to host programming commands by programming data in one of two designated blocks depending at least in part upon a number of host units of data specified by the host programming commands that have sequential logical addresses (paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate an example of Conley storing data with sequential logical addresses).

As for claim 2, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

responding to host commands to write units of data having non-sequential logical addresses by writing the data with sequential physical addresses into a first designated block, and responding to host commands to write units of data having sequential logical addresses equal to or in excess of a given proportion of said given number by writing the data into a second designated block (paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is

equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages)). Also note Conley's system is designed to account for storing either sequential logically addressed data, or non-sequentially logically addressed data, as described in paragraph 0050, all lines. In other words, if the given amount of host data is smaller than the area remaining in a partially written block, it will be stored in the first block (regardless if the data has sequential or non-sequential logical address). If the data is excess of a proportion of that given amount (amount of memory available in the partial block), the data will be written to the second, newly allocated block, again irrespective of the sequence of the logical addresses.

As for claim 3, Conley teaches writing data to the first designated block as including writing a number of host units of data into the first designated block having sequential logical addresses less than said given number (referring again to paragraph 0062, the given number is based on the memory available within the partial block).

As for claim 4, Conley teaches the non-volatile memory cells as being organized into multiple sub-arrays, and said blocks of memory cells include memory cells of two or more of the sub-arrays (paragraph 0062, all lines, if the amount of host data does not exceed the size of one full block the data, two different sets of host writes can be stored uniquely in one block (i.e. each write is a unique sub-array of data within each block).

Also note Conley specifically teaches his memory system as including sub-arrays in paragraph 0010, lines 1-7).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

3/30/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

CEW